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(54) **TITLE OF THE INVENTION:**

Method of manufacturing a semiconductor device

(57) **ABSTRACT**

Problem to Be Solved: To repair the damage to the gate oxide film as a result of the plasma etching used to from a gate electrode and of the impurity-ion implantation performed to form an LDD during the manufacturing process of a transistor having an LDD structure.

Solution: After ion implantation is performed to form an LDD, fluorine is introduced into the gate oxide film, prior to the formation of sidewalls, by heating the substrate by means of a lamp heater in an environment containing fluoride. In this manner, the dangling bonds of silicon atoms in the area where damage has been sustained as a result of plasma etching or ion implantation are terminated with fluorine, to yield stable Si-F bonds. As a result, changes in the

threshold voltage or a reduction in the carrier mobility is suppressed by ensuring that the damage is turned into neither near-interface states nor hot-carrier traps during the injection of hot carriers.

CLAIMS

What is claimed is:

1. A method of manufacturing a semiconductor consisting of a field-effect insulating gate transistor having a lightly doped drain (LDD) structure, wherein a silicon substrate is heated by means of a lamp heater in an environment containing fluoride, carried out after the formation of a gate electrode and the ion implantation of the LDD with impurity, but prior to the formation of sidewalls.

2. A method of manufacturing a semiconductor device according to claim 1, wherein the fluoride decomposes at 1,200°C or less and does not contain carbon.

3. A method of manufacturing a semiconductor device according to claim 1, wherein the temperature of heating by means of a lamp is higher than the temperature at which the fluoride decomposes and is in the range of 900°C to 1,200°C.

DETAILED DESCRIPTION OF THE INVENTION

[0001]
Technical Field of the Invention: The present invention relates to semiconductor devices, in particular to a method of manufacturing a semiconductor device with enhanced tolerance to hot carriers.

[0002]
Description of Related Art: In recent years, much progress has been made in the microminiaturization of the structure of MOS semiconductor devices, whereas the operating voltage of the transistor has not changed. In light of this situation, in the case of integrated-circuit semiconductor devices, the electric field intensity of the depletion layer region near the drain region of the transistor continues to be on the increase. Consequently, in special cases where the lateral field of the interface of the silicon substrate with the gate oxide film is sufficiently large, carriers that are accelerated in the region of an especially intense field near the drain become ionized and collide with the crystalline lattice of the substrate, to produce electron-hole pairs. Normally, when the temperature (the temperature of the electron and the hole) of the accelerated charged-particle system in the high electric field region exceeds the lattice temperature, these charged particles in particular are called hot carriers and some of the hot carriers pass the barrier between the substrate silicon and the gate oxide film to become injected into the gate oxide film. In other words, in the case of the n-channel transistor, the implantation

of electrons takes place, whereas holes are implanted in the case of the p-channel transistor. These injected carriers form near-interface states between the silicon and the gate oxide film, or else they become caught by the charge traps in the oxide film to cause fixed-charge accumulation. This causes changes in the threshold voltage of the transistor or degradation of the carrier mobility, thus compromising the reliability of the semiconductor device.

[0003] In the past, attempts were made to prevent such loss of reliability that accompanies the microminiaturization of elements by introducing the LDD structure to the MOS transistor.

[0004] Fig. 1 shows a cross-sectional view of an n-channel transistor having an LDD structure. Here, an n^--type region 6 with a low impurity concentration is formed in the channel region near an n^+ layer 7, which constitutes a drain region, in order to moderate the concentration of the lateral electrical field. Normally, the n^--type region 6 is formed prior to the formation of the n^+-type region 7 of the source and drain. In that case, an insulating layer 5, called a sidewall, is formed along the sides of a gate electrode 4 in advance during the process of implanting impurity before n^+-type region 7 is formed in order to prevent the impurity from being implanted into the already-formed n^--type region 6.

[0005] The method of manufacturing the MOS transistor having the LDD structure will be described hereinafter with reference to the accompanying diagrams. Fig. 2 and Fig. 3 illustrate the process sequence of one of the methods used to manufacture the MOS transistor. As shown in Fig. 2(a), a field oxide film 3 for isolating the element and a p^+ region 8, which serves as a stopper region, are first formed on a p-type substrate 1 using publicly known methods. Then, a gate oxide film 2 is formed on the p-type substrate 1 lying within the element region, and this is followed by the formation of a conductive film 11 comprised of a single layer of polycrystalline silicon containing such substances as phosphorus or, of a composite film made of polycrystalline silicon and a metal silicide having a high melting point.

[0006] A mask 12 is then formed on the conductive film as shown in Fig. 2(b), a gate electrode 4 is then formed by removing the conductive film lying outside the channel region using a publicly known etching technique. In cases where a micro-sized element is to be formed, a highly anisotropic method such as reactive ion etching (RIE) is used.

[0007] As shown in Fig. 3(a), an n^- layer 6 is formed by injecting an n-type impurity to self-align using the gate electrode 4 as the mask. Then, a silicon oxide film 9 is deposited on the entire surface of the element using the chemical vapor deposition (CVD) method.

[0008] As shown in Fig. 3(b), the silicon oxide film is etched using an anisotropic chemical etching method so that what remains on the sides of the gate electrode 4 constitute the sidewalls 5. In order to prevent damage to the exposed surface of the silicon substrate, a thin silicon oxide film 13 is then deposited on the entire surface of the element using a method such as CVD. Next, using the gate electrode 4 and the sidewalls 5 as the mask, ion implantation is performed using a high concentration of a self-aligned n-type impurity such as arsenic or phosphate [to form an n^+ layer 7], and the n^- layer 6 and the n^+ layer 7 are activated by heating in

a nitrogen environment at a high temperature. In this manner, the structure shown in Fig. 1 is obtained.

[0009]
Problems to be Solved by the Invention: With the above method of forming the LDD structure, when at the end of the etching of the material used to form the electrode during the formation of the gate electrode, the gate oxide film covering the surface of the region forming the n^- layer 6 becomes exposed to the plasma used for etching. This causes damage, such as the creation of near-interface states in the boundary between the oxide film and the silicon substrate or charge traps in the gate oxide film. Moreover, this region sustains further similar damage* caused by the energy of the ion implantation used to form the n^- layer. As for the charge traps in the film, trivalent silicon in the oxide film is considered to be the cause. Moreover, the near-interface states are caused by the dangling bonds resulting from the cleavage of the bonding of atoms between the oxide film and silicon, and they cause a decline in the mobility of the channel conduction carriers and behave like charge traps. During the subsequent heat treatment process, these defects from damage form Si-H bonds with hydrogen, which has been mixed into the treatment device. These bonds cannot be detected by electrical means at the stage when the fabrication of the device is completed. However, they are severed readily when hot carriers are injected, to become near-interface states or charge traps. For this reason, although the use of the LDD structure is considered to supress this, reduced carrier mobility due to the creation of near-interface states and changes in threshold voltage due to the trapping of charges take place when hot carriers, generated in more than a small quantity, are injected.

[0010] One conceivable means of removing the above defects is to remove the exposed surface of the gate oxide film using the etching method after the process of impurity-ion injection is carried out for forming the n^- layer, and to form a new oxide film on the surface of the silicon substrate using the thermal oxidation method. However, this is not a desirable method since it causes unevenness on the surface of the silicon substrate at the gate terminal area.

[0011] High-temperature heat treatment in an inert environment such as nitrogen is another means used to reverse the above damage without removing the gate oxide film. However, the damage cannot be repaired sufficiently with the use of this method alone.

[0012]
Means for Solving the Problems: The present invention provides the following: after the ion-implantation process for forming the n^- layer of the LDD structure, it is heated by means of a lamp annealer in an environment containing a fluoride that decomposes at 1,200°C or less and does not contain carbon, such as sulphur hexafluoride (SF_6), which decomposes at 400°C, or nitrogen trifluoride (NF_3), which decomposes at 500°C, at the temperature at which the fluoride decomposes or higher and between 900°C – 1,200°C.

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* Translator's note: Typographical error in the original text assumed.

[0013] With this method, the oxide film contains fluorine that exists in the form of Si-F bonds. Because of this, near-interface states at the boundary of the oxide film and silicon substrate, i.e., dangling silicon bond, are terminated by fluorine so that they do not act as near-interface states. Furthermore, because Si-F bonds are very stable, they are not severed by the injection of hot carriers, nor does the degradation of the carrier mobility that accompanies the increase in near-interface states take place. Likewise, because the charge traps in the oxide film, i.e., dangling trivalent silicon bonds, are terminated by fluorine, they no longer trap charges, nor are they severed by the injection of hot carriers, thus inhibiting fluctuations in the threshold voltage.

[0014] In this manner, the trapping of hot carriers injected while the device is in operation and the creation of near-interface states are both suppressed by the introduction of fluorine into the oxide film by the application of heat treatment by means of a lamp, thereby improving the reliability of the device.

[0015] In this case, the use of a temperature in excess of 1,200°C for the heat treatment will have the reverse effect of compromising the reliability of the device, because more traps will be generated.

[0016] Moreover, the presence of carbon in the environment of the heat treatment causes carbon to enter the oxide film. Since this reduces the pressure tightness of the oxide film, the use of fluorides that contain carbon should be avoided.

[0017] Furthermore, the use of the heat-resistant type quartz furnace, which is the usual means of applying heat treatment, requires a long treatment in order to introduce fluoride into the oxide film. As a result, the core pipe becomes eroded by hydrogen fluoride (HF) produced by the reaction of the fluoride with hydrogen entering the furnace from the atmosphere. On the other hand, the use of a lamp-heat type annealer allows for fluorine to be introduced into the oxide film by heat treatment applied for a short period of time. Therefore, there is no danger of the furnace becoming eroded.

[0018] Moreover, because fluorides such as sulphur hexafluoride and nitrogen trifluoride are very stable at room temperature, they have the advantage that they are easy to store.

[0019]
Description of the Preferred Embodiments: A first embodiment of the present invention will be described in detail hereinafter.

[0020] Fig. 1 is a cross-sectional view of an MOS transistor having an LDD structure, while Fig. 2 and Fig. 3 are diagrams illustrating the sequence of the steps used to manufacture the transistor of Fig. 1.

[0021] Firstly, as shown in Fig. 2(a), a field oxide film 3 for isolating the element and a p^+ region 8, which is to serve as a stopper region, are formed on a p-type silicon substrate 1 using a publicly known technology. Then, a gate oxide film 2 is formed on the p-type substrate 1 inside

the element region, followed by the formation of a conductive film 11 consisting of a single layer of polycrystalline silicon containing substances such as phosphate or of a composite film made up of polycrystalline silicon and a silicide of a metal having a high melting point.

[0022] Next, a mask 12 is formed on a conductive film, and a gate electrode 4 is formed by removing the conductive film lying in the area outside the channel region using a publicly known etching technique as shown in Fig. 2(b). In cases where a micro-sized element is to be formed, a highly anisotropic method such as reactive ion etching (RIE) is used.

[0023] In the case of the conventional manufacturing method, a silicon oxide film is deposited on all sides of the element using the CVD method, as shown in Fig. 3(a). In this embodiment of the present invention, however, fluorine is introduced into the gate oxide film 2 prior to the formation of the silicon oxide film in order to repair the damage sustained by the gate oxide film 2 lying on the n^- layer caused by etching used to form the gate electrode and by the ion implantation used to form the n^- layer. This is accomplished by introducing, into a lamp annealer, a carbon-free fluoride, which decomposes at 1,200°C or less, such as sulphur hexafluoride, which decomposes at 400°C, and by heating at 1,000°C for one minute.

[0024] Figure 4 is a cross-sectional view of a lamp annealer. The silicon substrate 23 is fixed on a quartz support 24 inside a quartz chamber 21. Its constitution is such that the silicon substrate 23 is heated by a halogen lamp 22 by feeding an ambient gas 26 to the interior of the chamber 21.

[0025] The depth profiles of the fluorine, silicon and oxygen concentrations in the oxide film after the heat treatment by means of a lamp, as determined by the Auger spectroscopy, are shown in Fig. 5. The abscissa shows the sputtering time required to expose the deep interior of the samples using argon, and it is nearly proportional to the depth from the surface. The interface of the gate oxide film and the silicon substrate was determined at a sputtering time of about 420 seconds. The diagram shows that the distribution of fluoride concentration is particularly high at the interface of the substrate silicon with the gate oxide film. Fluoride in the oxide film mainly exists in the form of Si-F and repairs the damage such as near-interface states and charge traps in the film.

[0026] Next, the structure shown in Fig. 1 is obtained by following the steps similar to those used by the conventional manufacturing method. In other words, a silicon oxide film is deposited on the entire surface of the element using the CVD method.

[0027] As shown in Fig. 3(b), the silicon oxide film 9 is etched using an anisotropic chemical ion etching method by leaving intact the portion on the sides of the gate electrode 4, to form sidewalls 5. A thin silicon oxide film 13 is then deposited on the entire surface of the element using, for example, the CVD method in order to prevent damage to the surface of the exposed substrate caused by the energy of ion implantation. Using the gate electrode 4 and the sidewall 5 as the mask, a highly concentrated n-type impurity such as arsenic or phosphate is ion implanted in a self-aligned manner. Then, an n^- layer and an n^+ layer are formed by activating the ion-

implanted layer, achieved by heating in an environment of high-temperature nitrogen, to obtain the structure shown in Fig. 1.

[0028] The effects of the introduction of fluorine will be demonstrated next by comparing the MOS transistor having an LDD structure prepared according the manufacturing method of the present invention with that prepared according to the conventional method. Fig. 6 shows changes (Δg_m) in mutual conductance (g_m) over time after the application of stress under conditions yielding maximum gate current. The changes in the mutual conductance reflect the decline in the carrier mobility that accompanies the generation of near-interface states as a result of the injection of hot carriers. The diagram shows that the Δg_m of the transistor manufactured according to the method of the present invention is lower than Δg_m of the one manufactured according to the conventional method. This shows that the use of the manufacturing method of the present invention has substantially improved the hot-carrier tolerance of the MOS transistor.

[0029] In the present embodiment, the n-channel transistor was used as an example. However, similar effects were also obtained with the p-channel transistor.

[0030] A second embodiment of the present invention will be described hereinafter.

[0031] With the present embodiment, after the gate electrode is etched and after the ion implantation for forming the n^- layer is performed, the silicon substrate is fixed inside a lamp annealer and heated under conditions, such as at 900°C for 2 minutes, using a supply of trivalent* [sic] nitrogen gas, which decomposes at 500°C.

[0032]
Advantages of the Invention: As described above, the present invention provides substantial improvement in the reliability of the device. This is achieved by the following: after the low-concentration impurity diffused layer of the LDD structure is formed, fluorine is introduced into the gate oxide, where near-interface states or charge traps have been created as a result of the etching plasma used to form the gate electrode or ion implantation used to form the n^- layer of the LDD structure. This is achieved by heating in an environment comprised of a carbon-free fluoride, which decomposes at a temperature of 1,200°C or less, by means of a lamp annealer at a temperature that is higher than the temperature at which the fluoride decomposes and between 900°C to 1,200°C, thereby terminating the unpaired end of silicon.

[0033] Furthermore, because heating using a lamp annealer raises only the temperature of the substrate, only a small of amount of fluoric acid is generated as a result of the reaction of the fluoride with hydrogen that gets mixed into the furnace, this offers the advantage in that the furnace is eroded only slightly.

[0034] Moreover, because hydrogen hexafluoride and nitrogen trifluoride are both very stable

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* Translator's note: Probably "nitrogen trifluoride" is intended.

at room temperature, there is another advantage in that they can be stored easily.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional view of an MOS transistor having an LDD structure.

Figs. 2(a) and (b) illustrate one sequence of the steps employed to manufacture the structure shown in Fig. 1.

Figs. 3(a) and (b) illustrate one sequence of the steps employed to manufacture the structure shown in Fig. 1.

Fig. 4 is a sectional view of a lamp annealer used to introduce fluorine according to the manufacturing method of the present invention.

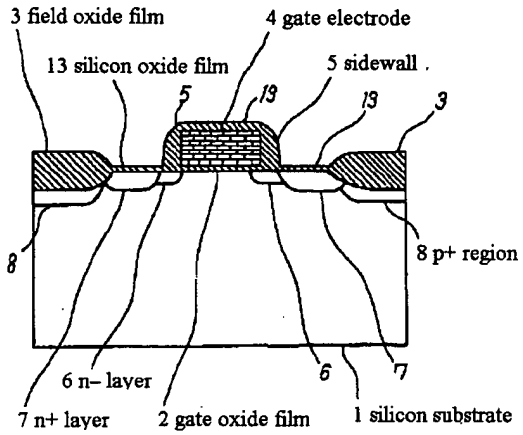
Fig. 5 is a graph showing the depth profiles for the concentrations of fluoride introduced into the oxide film, and silicon and oxygen both of which are present in the oxide film, respectively, according to the manufacturing method of the present invention.

Fig. 6 is a graph showing the stress-time dependence of the fluctuations in the charge mobility of an MOS transistor manufactured according to the manufacturing method of the present invention.

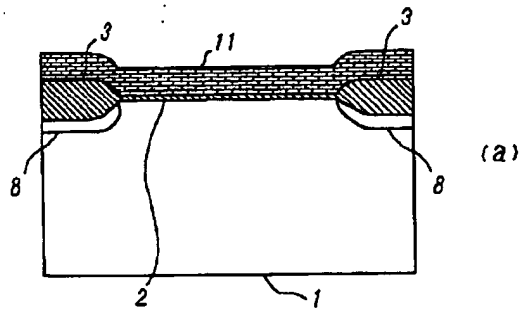
Description of the Reference Numerals

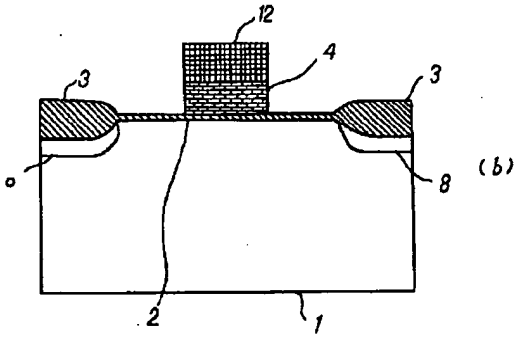
1. silicon substrate
2. gate oxide film
3. field oxide film
4. gate electrode
5. sidewall
6. n^- layer
7. n^+ layer
8. p^+ region
9. silicon oxide film
11. conductive film
12. mask
13. silicon oxide film
21. quartz chamber
22. halogen lamp
23. silicon substrate
24. support
25. main body
26. ambient gas

【図１】

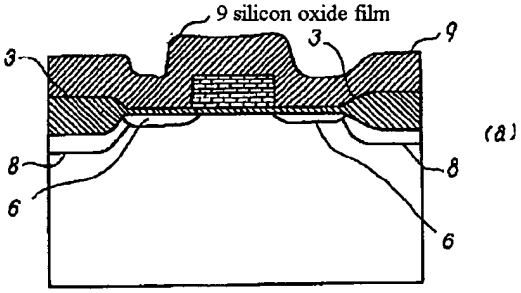

3 field oxide film
4 gate electrode
13 silicon oxide film
5 sidewall
8 p+ region
6 n− layer
7 n+ layer
2 gate oxide film
1 silicon substrate

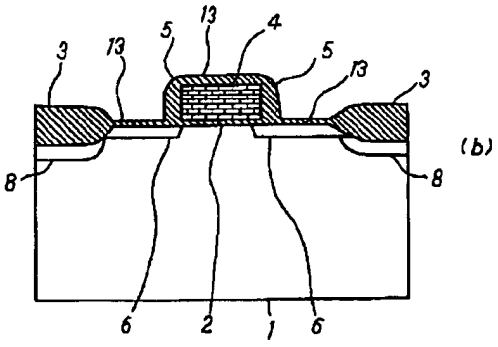
【図２】


(a)

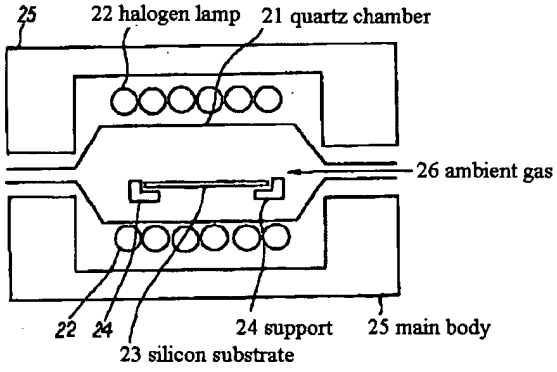

(b)

【図３】

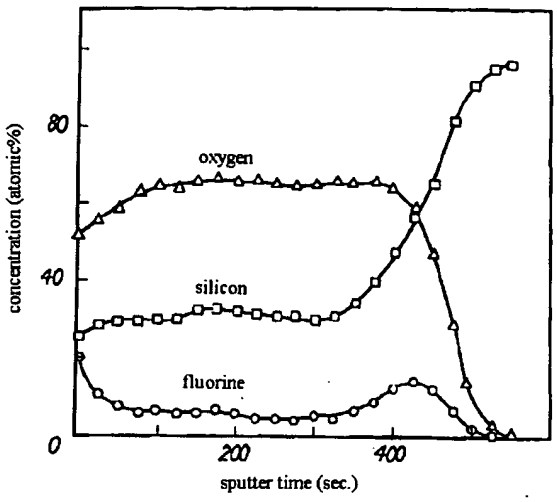

9 silicon oxide film
(a)


(b)

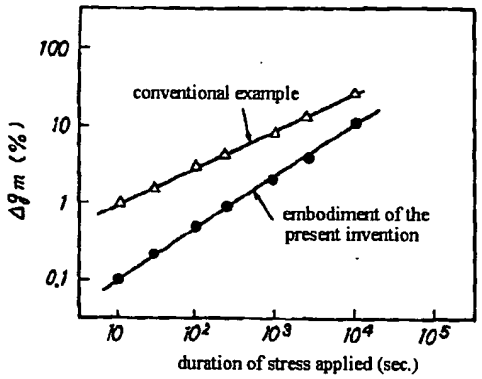
【図４】


22 halogen lamp
21 quartz chamber
26 ambient gas
24 support
25 main body
23 silicon substrate

【図5】


concentration (atomic%)
80
40
0
oxygen
silicon
fluorine
200
400
sputter time (sec.)

【図6】


100
10
1
0.1
Δgm (%)
conventional example
embodiment of the present invention
10
10²
10³
10⁴
10⁵
duration of stress applied (sec.)